REMARKS/ARGUMENTS

Claims 1, 7-12, 17 and 18 are pending. Claim 18 is cancelled.

Claim 1 is amended to comprise limitation "the conductive traces are formed from electrically conductive layers as a whole on the core layer by pattering", which is taught on page 11, lines 3-8 and supported by FIGS. 3A-4B. Claim 12 is amended to eliminate the limitation "the method is used for a electronic device mounted with the library core" and to comprise limitation "the electrically conductive layers formed as a whole on the core layer are over the upper and lower surfaces of the core layer respectively", which is taught on page 11, lines 3-8 and supported by FIGS. 3A-4B. Two new claims 19 and 20 are added according to the description of the present application on page 10, third paragraph. No new matter is introduced by these amendments. Approval of the amendments to claims 1 and 12 is respectfully requested.

Claims 1 and 7-10 are rejected by the Examiner under 35 U.S.C 102(e) as being anticipated by Kimura et al. (US 6,806,428), which is referenced as citation 1 hereinafter. Claim 11 is rejected by the Examiner under 35 U.S.C 103(a) as being unpatentable over citation 1 in view of Okabe et al. (US 6,757,178), which is referenced as citation 2 hereinafter. Claims 12 and 17 are rejected by the Examiner under 35 U.S.C 103(a) as being unpatentable over citation 1.

Rejections under 35 U.S.C. § 102

The rejection of claims 1 and 7-10 as anticipated by Kimura et al. (citation 1) is respectfully traversed. As shown in FIGS. 6(a)-6(i), citation 1 teaches to form through holes (33) by drill or laser to penetrate through a resin substrate (31) of which both sides are lined with copper foils (32) so as to form conductive vias in the resin substrate (31) for electrically connecting the two copper foils (32). Then, by using a photolithographic technology to pattern the copper foils (32), desired circuit wiring patterns (34) are formed on both sides of resin substrate (31). Next, penetration holes (35) are formed for ***inserting*** *chip components* as chip resistors (36) and chip capacitors (37), wherein each of the chip resistors (36) and the chip

capacitors (37) comprise two end electrodes (36a or 37a) respectively formed on the ends of the chip (36 or 37). Then, conductive resins are applied or printed on end electrodes (36a and 37a) to form connection electrodes (38) as shown in FIG. 6(g) so that the end electrodes (36a and 37a) are capable of electrically connecting with the circuit wiring patterns (34).

To the contrary, the present application teaches to form openings (32) in the core layer (31) beforehand, and then to ***fill*** the openings (32) with capacitive materials. Next, electrically conductive layers (34) are formed as a whole on the core layer (31) and the capacitive materials. Then, the electrically conductive layers (34) are patterned to form conductive traces (34a). The conductive traces (34a) are capable of electrically connecting with the capacitive materials and are partly used as parallel sheets (34c) onto the capacitive materials to form capacitors (33b) embedded in the core layer (31).

Regarding the rejection of claim 1, the differences between citation 1 and the amended claim 1 of the present application include:

(a) Citation 1 provides a resin substrate (31) of which both sides are lined with copper foils (32), and the present application provides a core layer (31) with electrically conductive layers (34) that are formed as a whole on *the core layer (31)* and *the capacitive materials*. Therefore, the bases provided by citation 1 and the present application are not identical.

(b) Citation 1 teaches to form the circuit wiring patterns (34) by patterning the copper foils (32) on the both sides of the resin substrate (31), and to form the penetration holes (35) ***later***. However, the present application has disclosed that the openings (32) in the core layer (31) is formed ***prior to*** forming the electrically conductive layers (34) because the capacitive materials, which are filled within the openings (32), are covered by the electrically conductive layers (34) as shown in FIG. 3B.

(c) Citation 1 teaches to ***insert*** the chip resistors (36) and the chip capacitors (37) to the penetration holes (35), and the present application teaches to ***fill*** the openings (32) with capacitive materials. Therefore, the materials inserted to the penetration holes (35) disclosed by citation 1 is different from the capacitive materials as recited in claim 1 of the present application.

According to the specification, citation 1 teaches that after forming the through holes (33) through the resin substrate (31) of which both sides are lined with copper foils (32), forming the conductive vias in the resin substrate (31) to electrically connect the two copper foils (32). Then, the circuit wiring patterns (34) are formed on both sides of resin substrate (31) by patterning the copper foils (32). Next, the ***chip*** resistors (36) and the ***chip*** capacitors (37) are ***inserted*** into the penetration holes (35). Then, the conductive resins are applied or printed on the end electrodes (36a and 37a) to form the connection electrodes (38) as shown in FIG. 6(g) so that the end electrodes (36a and 37a) are capable of electrically connecting with the circuit wiring patterns (34). However, the present application teaches to form openings (32) in the core layer (31) ***prior to*** forming the electrically conductive layers (34), which are formed as a whole on the core layer (31) and the capacitive materials. Then, the electrically conductive layers (34) are patterned to form the conductive traces (34a), which electrically connecting with the capacitive materials and partly used as parallel sheets (34c) onto the capacitive material to form capacitors (33b). To the contrary, citation 1 teaches to use the connection electrodes (38) to connect the passive components with the circuit wiring patterns (34). Therefore, the structure of the claimed library core (3) of the present application is totally different from that disclosed by citation 1 so that claim 1 is not anticipated by citation 1.

In addition, the passive components disclosed by citation 1 are the ***chip*** resistors (36) and the ***chip*** capacitors (37), which comprise electrode 36a and 37a. To the contrary, the passive components disclosed by the present application are made of the capacitive materials, which do

not have a constant shape. After filling the capacitive materials into the opening (32) in the core layer (31), the electrically conductive layers (34) are formed as a whole on the core layer (31). Then, the electrically conductive layers (34) are patterned to form conductive traces (34a), which are partly used as parallel sheets (34c) onto the capacitive materials to form capacitors (33b). It can be understood that the parallel sheets (34c) of the capacitors (33b) and the conductive traces (34a) are located in the same circuit layer. Therefore, the structure of the claimed library core (3) of the present application is further different from that disclosed by citation 1 so that claim 1 is not anticipated by citation 1.

Regarding the rejection of claim 7, citation 1 does teach to form the through holes (33) in the resin substrate (31) of which both sides are lined with copper foils (32). Then, non-electric copper plating is applied to conduct between both copper foils (32), i.e. FIG 6(c): through-hole plating step. However, since citation 1 fails to disclose the features "filling the openings (32) with capacitive materials to form the capacitors (33b)" and "the conductive traces (34a) and the parallel sheets (34c) are located ***in the same circuit layer***", as recited or suggested in claim 1. Therefore, claim 7, which is dependent on claim 1, is not anticipated by citation 1.

Regarding the rejection of claim 8, citation 1 does disclose that the library core (3) with inserted chip components (36 and 37) and the circuit wiring patterns (34) can be formed on a substrate or a printed circuit board. However, since citation 1 fails to disclose the features "filling the openings (32) with capacitive materials to form the capacitors (33b)" and "the conductive traces (34a) and the parallel sheets (34c) are located ***in the same circuit layer***", as recited or suggested in claim 1. Therefore, claim 8, which is dependent on claim 1, is not anticipated by citation 1.

Regarding the rejection of claim 9, as shown in FIGS. 1(a) and 1(b), citation 1 teaches that chip resistors (2), chip capacitors (3), and other chip components are ***inserted*** into

penetration holes having the nearly same hole shapes as chip components, and their end electrodes and circuit wirings (4a and 4b) formed on both sides of resin substrate (1) are electrically coupled to compose a desired electric circuit. To the contrary, the present application teaches to ***fill*** the openings (32) with capacitive materials to form the capacitors (33b). Therefore, the bases of citation 1 and the present application for forming a multi-layer circuit board are different. Moreover, citation 1 fails to disclose the feature "the conductive traces (34a) and the parallel sheets (34c) are located ***in the same circuit layer***", as suggested in claim 1. Therefore, claim 9, which is dependent on claim 1, is not anticipated by citation 1.

Regarding the rejection of claim 10, as shown in FIGS. 1(a) and 1(b), citation 1 does disclose that an IC chip (7) mounted on the multi-layer circuit board and electrically coupled to the conductive traces (4a, 4b, and 4c). The multi-layer circuit board with mounted IC chip (7) is inherently a fabrication in a flip-chip semiconductor packaging substrate. However, since citation 1 fails to disclose the features "filling the openings (32) with capacitive materials to form the capacitors (33b)" and "the conductive traces (34a) and the parallel sheets (34c) are located ***in the same circuit layer***", as recited or suggested in claim 1. Therefore, claim 10, which is dependent on claim 1, is not anticipated by citation 1.

Rejections under 35 U.S.C. § 103

The rejections of claims 11, 12 and 17 as obvious over citation 1 alone, or in view of Okabe et a. (citation 2), are respectfully traversed.

Regarding the rejection of claim 11, citation 2 does disclose that a transmission-line conductor (50) is connected to the front-surface conductor (15a), and that the transmission-line conductor (50) is connected via a bonding wire (41a) to a pad (42a) provided on a semiconductor element (40). However, since citations 1 and 2 fail to disclose the features "filling the openings (32) with capacitive materials to form the capacitors (33b)" and "the conductive traces (34a) and

the parallel sheets (34c) are located ***in the same circuit layer***", as recited or suggested in claim 1. Therefore, claim 11, which is dependent on claim 1, is not anticipated by citation 1.

In addition, according to specification of the present application, the materials for passive components embedded in the insulating core layer (31) can be adapted to be formed with parallel and/or series electrical connection between the capacitors (33b); and, capacitance of the capacitors (33b) can be determined upon types and quantities of the materials for the capacitors (33b) filled into the openings (32) of the core layer (31). However, citations 1 and 2 fail to teach such features.

Regarding the rejection of claim 12, the differences between citation 1 and the amended claim 12 of the present application include:

(a) Citation 1 provides a resin substrate (31) of which both sides are lined with copper foils (32), and the present application provides a core layer (31) with electrically conductive layers (34) that are formed as a whole on *the core layer (31)* and *the capacitive materials*. Therefore, the bases provided by citation 1 and the present application are not the same.

(b) Citation 1 teaches to form the circuit wiring patterns (34) by patterning the copper foils (32) on the both sides of the resin substrate (31), and to form the penetration holes (35) ***later***. However, the present application has disclosed that the openings (32) in the core layer (31) is formed ***prior to*** forming the electrically conductive layers (34) because the capacitive materials, which are filled within the openings (32), are covered by the electrically conductive layers (34) as shown in FIG. 3B. The method recited in claim 12 is different from that of citation 1.

(c) Citation 1 teaches to ***insert*** the chip resistors (36) and the chip capacitors (37) to the penetration holes (35), and the present application teaches to ***fill*** the openings (32)

with capacitive materials. Therefore, the method recited in claim 12 is different from that of citation 1.

(d) According to the specification of the present application, the electrically conductive layers (34) are formed after the openings (32) are formed in the core layer (31). However, initially, citation 1 provides a double-side copper lined substrate without performing any process beforehand. Therefore, the method recited in claim 12 is different from that of citation 1.

(e) Citation 1 teaches to form the circuit wiring patterns (34) on both sides of resin substrate (31) by patterning the copper foils (32). Next, the penetration holes (35) are formed for inserting the chip resistors (36) and chip capacitors (37). Then, conductive resins are applied or printed on the end electrodes (36a and 37a) to form connection electrodes (38) as shown in FIG. 6(g) to electrically connect the end electrodes (36a and 37a) with the circuit wiring patterns (34). Oppositely, the present application teaches to form the electrically conductive layers (34) as a whole on the core layer (31) and the capacitive materials after filling the openings (32) with capacitive materials. Then, the electrically conductive layers (34) are patterned to form conductive traces (34a). <u>The conductive traces (34a) are electrically connecting with the capacitive materials and partly used as parallel sheets (34c) onto the capacitive material to form capacitors (33b)</u>. Therefore, the conductive traces (34a) and the parallel sheets (34c) are formed ***simultaneously*** by performing a ***single*** patterning process. However, in citation 1, conductive resins are applied or printed on the end electrodes (36a and 37a) to form the connection electrodes (38). In such case, it requires higher accuracy for alignment when performing the applying or printing conductive resin procedure, which results in raising the complexity of manufacture processes. Since the conductive traces (34a) according to the present application are capable of electrically connecting with the capacitive materials without forming the connection electrodes (38) as citation 1, the manufacture processes according to the

present application can be simplify and the fabrication cost can be reduced. Therefore, the examiner's alleged combination cannot render the method of the present invention obvious. Therefore, the examiner's rejection of claim 12 is not justified.

Regarding the rejection of claim 17, citation 1 teaches to form the through holes (33) in the resin substrate (31) of which both sides are lined with copper foils (32). Then, non-electric copper plating is applied to conduct between both copper foils (32), i.e. FIG 6(c): through-hole plating step. However, since citation 1 fails to disclose the features "<u>filling the openings (32) with capacitive materials to form the capacitors (33b)</u>" and "<u>the conductive traces (34a) and the parallel sheets (34c) are formed simultaneously</u>", as recited or suggested in claim 12. Since claim 17 is dependent on claim 12, and it should be patentable.

<u>Response to Examiner's Comments</u>

With respect to the Examiner's response to Applicant's Dec. 15, 2005 arguments, Applicant responds as follows:

(a) The examiner suggests the step in which citation 1, i.e. forming the wiring pattern before forming the holes and the inserting passive chips while the applicant forms the substrate with holes first before forming the wring pattern, is not necessitating when the final product is being made. However, the connection electrodes (38) disclosed by citation 1 must be formed on the electrodes (36a and 37a) to connect the passive components with the circuit wiring patterns (34) because the chip resistors (36) and the chip capacitors (37) are inserted into the penetration holes (35) after forming the circuit wiring patterns (34) on both sides of the resin substrate (31). Therefore, the structure of the library core and the method for the library core according to the present application are different from those of citation 1.

(b) The examiner suggests claims 1 and 12 do not state the limitation "the conductive layers formed as a whole on the core layer". Therefore, claims 1 and 12 are amended to include such limitation. Furthermore, two new claims 19 and 20 are added to define the scope of the capacitive materials as recited in claims 1 and 12.

In view of the foregoing amendments and remarks, Applicant submits that the present application is in condition for allowance. A Notice of Allowance is therefore respectfully requested.

Applicant hereby submits its request for a two month extension of time. The Commissioner is hereby authorized to charge the fees for a two month extension of time to Deposit Account No. 50-0337.

The Commissioner is hereby authorized during prosecution of this application to charge any fees that may be required (except for patent issue fees required under 37 CFR §1.18) or to credit any overpayment of fees to Deposit Account No. 50-0337.

Dated: September 15, 2006

Respectfully submitted,

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